

Figure 4.10 RTL Schematic for Full adder

Step 2: Write the testbench code for full adder and obtain the RTL simulation waveform Testbench code:

```
module tb_top;

reg a, b, c;

wire s, c_out;

full_adder fa(a, b, c, s, c_out);

initial begin

Smonitor("At time %0t: a=%b b=%b, cim=%b, sum=%b, carry=%b",Stime, a,b,c,s,c_out);

a = 0; b = 0; c = 0; #1;

a = 0; b = 1; c = 0; #1;

a = 0; b = 1; c = 0; #1;

a = 0; b = 1; c = 0; #1;
```

Microprocessors Lab Manual Vtu

SJ Ball

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