

Chrysostomos Nicopoulos
Vijaykrishnan Narayanan
Chita R. Das

Network-on-Chip Architectures

A Holistic Design Exploration

Network On Chip Architectures A Holistic Design Exploration Lecture Notes In Electrical Engineering

**Anastasia Barger, Tekhniyon, Makhon
tekhnologi le-Yisra'el. Fakultah le-
handasat hashmal**

Network On Chip Architectures A Holistic Design Exploration Lecture Notes In Electrical Engineering:

Network-on-Chip Architectures Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R. Das, 2009-09-18 2 The Cell Processor from Sony Toshiba and IBM STI 3 and the Sun UltraSPARC T1 formerly codenamed Niagara 4 signal the growing popularity of such systems Furthermore Intel s very recently announced 80 core TeraFLOP chip 5 exemplifies the irreversible march toward many core systems with tens or even hundreds of processing elements 1 2 The Dawn of the Communication Centric Revolution The multi core thrust has ushered the gradual displacement of the computation centric design model by a more communication centric approach 6 The large sophisticated monolithic modules are giving way to several smaller simpler processing elements working in tandem This trend has led to a surge in the popularity of multi core systems which typically manifest themselves in two distinct incarnations heterogeneous Multi Processor Systems on Chip MPSoC and homogeneous Chip Multi Processors CMP The SoC philosophy revolves around the technique of Platform Based Design PBD 7 which advocates the reuse of Intellectual Property IP cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations The appeal of such a modular approach lies in the substantially reduced Time To Market TTM incubation period which is a direct outcome of lower circuit complexity and reduced design effort The whole system can now be viewed as a diverse collection of pre existing IP components integrated on a single die *The British National Bibliography* Arthur James Wells, 2009 Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures Umit Y. Ogras, Radu Marculescu, 2013-03-12 Traditionally design space exploration for Systems on Chip SoCs has focused on the computational aspects of the problem at hand However as the number of components on a single chip and their performance continue to increase the communication architecture plays a major role in the area performance and energy consumption of the overall system As a result a shift from computation based to communication based design becomes mandatory Towards this end network on chip NoC communication architectures have emerged recently as a promising alternative to classical bus and point to point communication architectures In this dissertation we study outstanding research problems related to modeling analysis and optimization of NoC communication architectures More precisely we present novel design methodologies software tools and FPGA prototypes to aid the design of application specific NoCs **Zooming in on Network-on-chip Architectures** Israel Cidon, Idit Keidar, 2005 **Performance and Energy Efficient Network-on-chip Architectures** Sriram R. Vangal, 2007 **Communication Architectures for Systems-on-Chip** José L. Ayala, 2018-09-03 A presentation of state of the art approaches from an industrial applications perspective Communication Architectures for Systems on Chip shows professionals researchers and students how to attack the problem of data communication in the manufacture of SoC architectures With its lucid illustration of current trends and research improving the performance quality and reliability of transactions this is an essential reference for anyone dealing with communication mechanisms for embedded systems systems on chip and multiprocessor architectures or trying to

overcome existing limitations Exploring architectures currently implemented in manufactured SoCs and those being proposed this book analyzes a wide range of applications including Well established communication buses Less common networks on chip Modern technologies that include the use of carbon nanotubes CNTs Optical links used to speed up data transfer and boost both security and quality of service QoS The book s contributors pay special attention to newer problems including how to protect transactions of critical on chip information personal data security keys etc from an external attack They examine mechanisms revise communication protocols involved and analyze overall impact on system performance

Low Power Networks-on-Chip Cristina Silvano,Marcello Lajolo,Gianluca Palermo,2010-09-24 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures

Network on Chip (NOC) Topologies - a Cost Minimization Design Approach Ehud Shavit,Ṭekhniyon, Makhon ṭekhnologi le-Yiśra'el. Fakultah le-handasat hashmal,2007 Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication Shen, Jih-Sheng,Hsiung, Pao-Ann,2010-06-30 Reconfigurable computing brings immense flexibility to on chip processing while network on chip has improved flexibility in on chip communication Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems on chip This book is the one of the first compilations written to demonstrate this future for network on chip design Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques to task assigning scheduling and arrival to designing an operating system to take advantage of the computing and communication flexibilities brought about by run time reconfiguration and network on chip it represents a complete source of the techniques and applications for reconfigurable network on chip necessary for understanding of future of this field *Design and Implementation of Low-latency, Low-power Reconfigurable On-chip Networks* Chia-Hsin Chen (Ph. D.),2017 In this dissertation I tackle large low latency low power on chip networks I focus on two key challenges in the realization of such NoCs in practice 1 the development of NoC design toolchains that can ease and automate the design of large scale NoCs paving the way for advanced ultra low power NoC techniques to be embedded within many core chips and 2 the design and implementation of chip prototypes that demonstrate ultralow latency low power NoCs enabling rigorous understanding of the design tradeoff of such NoCs I start off by presenting DSENT joint work a timing area and power evaluation toolchain that supports flexibility in modeling while ensuring accuracy through a technology portable library of standard cells 108 DSENT enables rigorous design space exploration for advanced technologies and have been shown to provide fast and accurate evaluation of emerging opto electronics Next low swing signaling has been shown to substantially reduce NoC power but requires custom circuit design in the past I propose a toolchain that automates the embedding of low swing cells into the

NoC datapath paving the way for low swing signaling to be part of future many core chips 17 Third clockless repeated links have been shown to be embeddable within a NoC datapath allowing packets to go from source to destination cores without being latched at intermediate routers I propose SMARTapp a design that leverages these clockless repeaters for configuration of a NoC into customized topologies tailored for each applications and present a synthesis toolchain that takes each SoC application as input and synthesize a NoC configured for that application generating RTL to layout 18 The thesis next presents two chip prototypes that I designed to obtain on depth understanding of the practical implementation costs and tradeoffs of high level architectural ideas The SMART NoC chip is a 3 x 3 mm² chip in 32 nm SOI realizing traversal of 7 hops within a cycle at 548 MHz dissipating 1.57 to 2.53 W It enables a rigorous understanding of the tradeoffs between router clock frequency network latency and throughput and is a demonstration of the proposed synthesis toolchain The SCORPIO 36 core chip joint work is an 11 x 13 mm² chip in 45 nm SOI demonstrating snoopy coherence on a scalable ordered mesh NoC with the NoC taking just 19 % of tile power and 10 % of tile area 19 28

On the Effects of Process Variation in Network-on-chip Architectures Chrysostomos Nicopoulos, 2007 Abstract The advent of diminutive technology feature sizes has led to escalating transistor densities Burgeoning transistor counts are casting a dark shadow on modern chip design global interconnect delays are dominating gate delays and affecting overall system performance Networks on Chip NoC are viewed as a viable solution to this problem because of their scalability and optimized electrical properties However on chip routers are susceptible to another artifact of deep submicron technology Process Variation PV PV is a consequence of manufacturing imperfections which may lead to degraded performance and even erroneous behavior In this work we present the first comprehensive evaluation of NoC susceptibility to PV effects and we propose an array of architectural improvements in the form of a new router design called SturdiSwitch to increase resiliency to these effects Through extensive re engineering of critical components SturdiSwitch provides increased immunity to PV while improving performance and increasing area and power efficiency

Low Power Networks-on-Chip Cristina Silvano, Marcello Lajolo, Gianluca Palermo, 2010-10-06 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures

Modeling and Design of Network on Chip Interconnects Anastasia Barger, Tekhniyon, Makhon tekhnologi le-Yiśra'el. Fakultah le-handasat hashmal, 2006

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